Data Sheet **January 2002**

3.0A, 100V, 1.200 Ohm, P-Channel Power MOSFET

This P-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17541.

Ordering Information

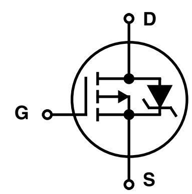
PART NUMBER	PACKAGE	BRAND
IRF9510	TO-220AB	IRF9510

NOTE: When ordering, include the entire part number.

Features

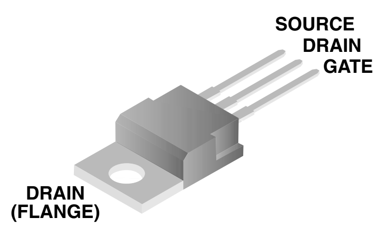
- 3.0A, 100V
- $r_{DS(ON)} = 1.200\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

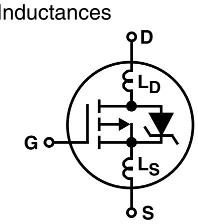
		IRF9510	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	-100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	-100	V
Continuous Drain Current	I_D	-3.0	A
$T_C = 100^oC$	I_D	-2.0	A
Pulsed Drain Current (Note 3)	I_{DM}	-12	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	20	W
Linear Derating Factor		0.16	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	190	mJ
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

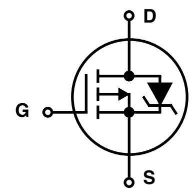
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$, (Figure 10)		-100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250\mu A$		-2.0	-	-4.0	V
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	±100	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $V_{GS} = 0V$		-	-	-25	µA
		$V_{DS} = 0.8$ x Rated BV_{DSS}, $V_{GS} = 0V$, $T_C = 125^oC$		-	-	-250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = -10V$, (Figure 7)		-3.0	-	-	A
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$V_{GS} = -10V$, $I_D = -1.5A$, (Figures 8, 9)		-	1.000	1.200	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, $I_D = -1.5A$, (Figure 12)		0.8	1.1	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5$ x Rated BV_{DSS}, $I_D \approx -3.0A$, $R_G = 50\Omega$, $V_{GS} = 10V$, (Figures 17, 18) $R_L = 15.7\Omega$ for $V_{DSS} = 50V$ $R_L = 12.3\Omega$ for $V_{DSS} = 40V$ MOSFET Switching Times are Essentially Independent of Operating Temperature		-	15	30	ns
Rise Time	t_r			-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	20	40	ns
Fall Time	t_f			-	20	40	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = -10V$, $I_D = -3A$, $V_{DS} = 0.8$ x Rated BV_{DSS}, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature		-	8.5	11	nC
Gate to Source Charge	Q_{gs}			-	3.8	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	4.7	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = -25V$, f = 1.0MHz, (Figure 11)		-	180	-	pF
Output Capacitance	C_{OSS}			-	85	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	30	-	pF
Internal Drain Inductance	L_D	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Junction to Case	$R_{\theta JC}$			-	-	6.4	$^oC/W$
Junction to Ambient	$R_{\theta JA}$	Typical Socket Mount		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	-3.0	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	-12	A
Source to Drain Diode Voltage(Note 2)	V_{SD}	$T_C = 25^oC$, $I_{SD} = -3.0A$, $V_{GS} = 0V$, (Figure 13)		-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = -3.0A$, $dI_{SD}/dt = 100A/\mu s$		-	120	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = -3.0A$, $dI_{SD}/dt = 100A/\mu s$		-	6.0	-	μC

NOTES:

2. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, $L = 31.7mH$, $R_G = 25\Omega$, peak $I_{AS} = 3.0A$. See Figures 15, 16.

Typical Performance Curves Unless Otherwise Specified

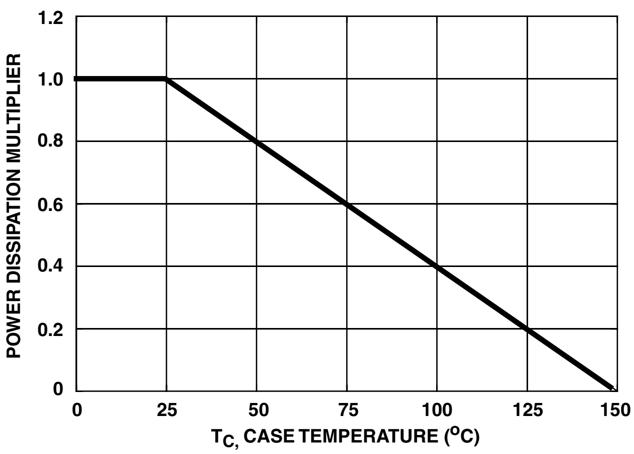


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

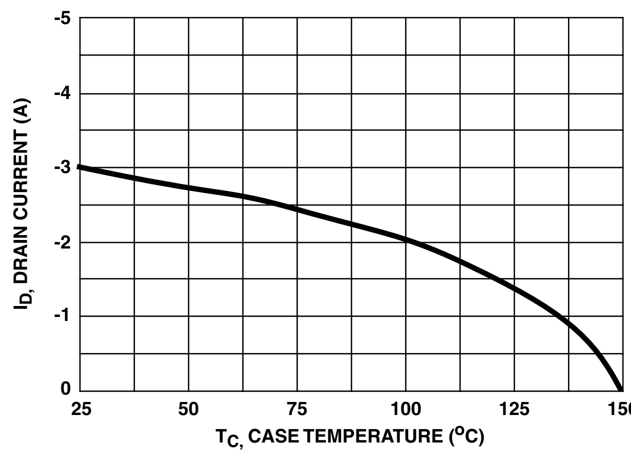


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

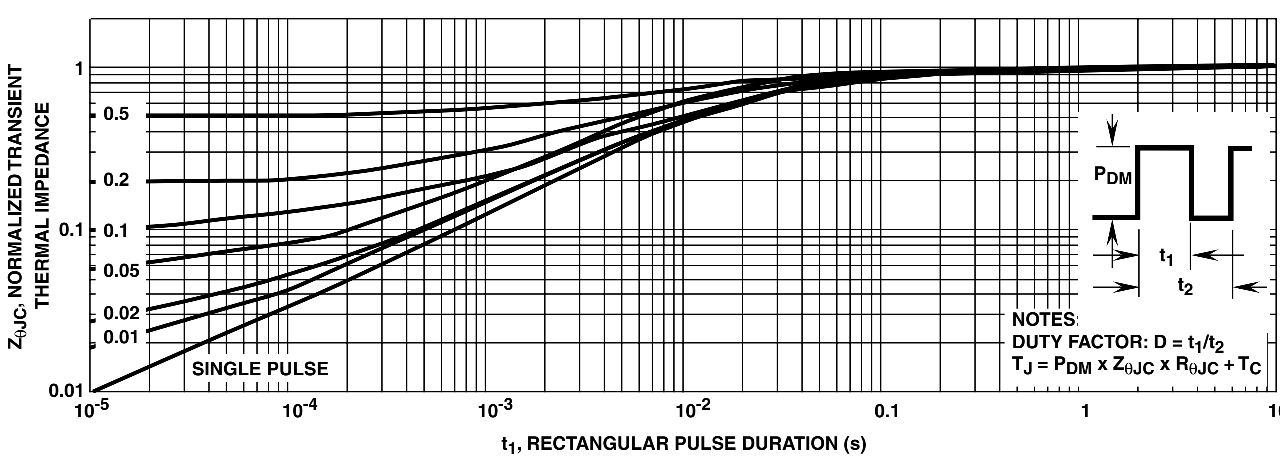


FIGURE 3. NORMALIZED TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

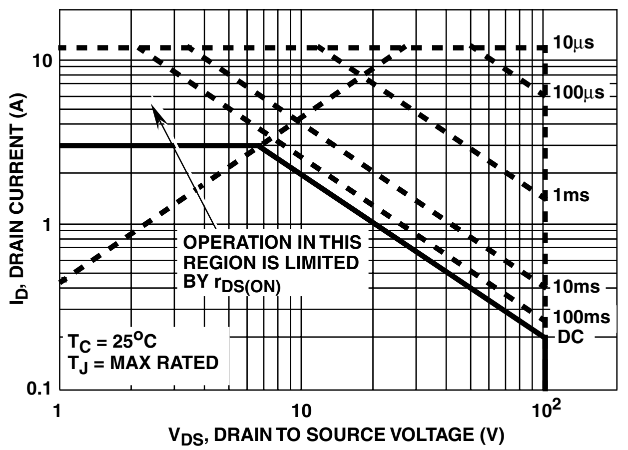


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

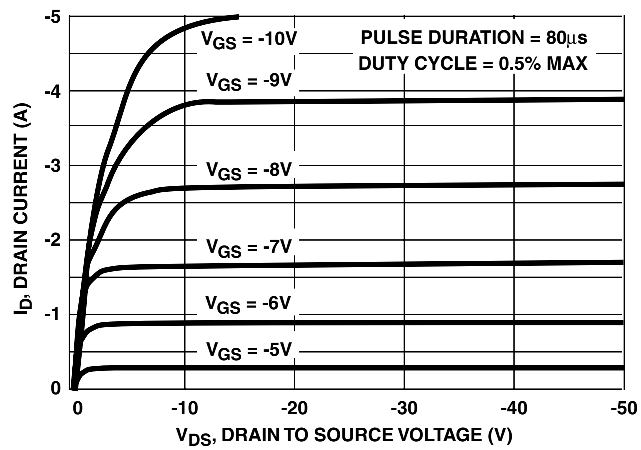


FIGURE 5. OUTPUT CHARACTERISTICS

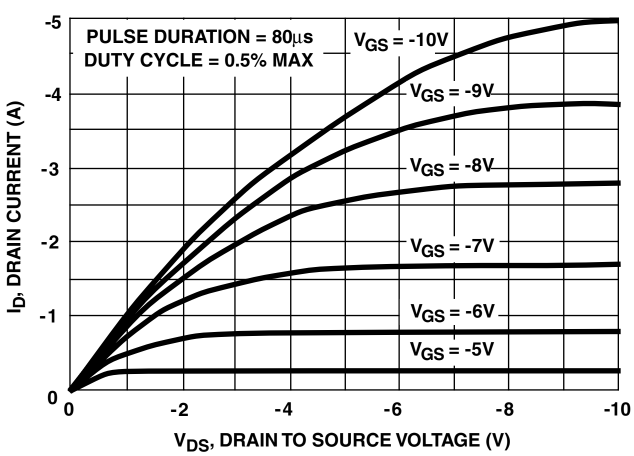


FIGURE 6. SATURATION CHARACTERISTICS

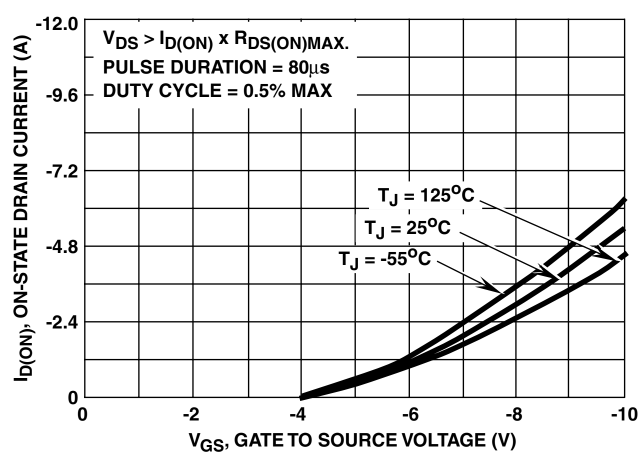


FIGURE 7. TRANSFER CHARACTERISTICS

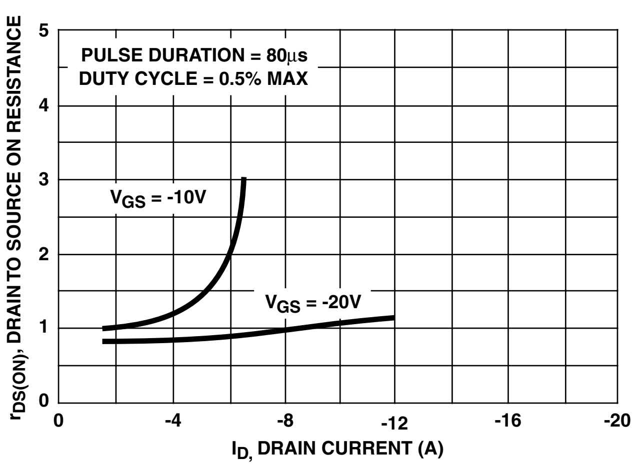


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

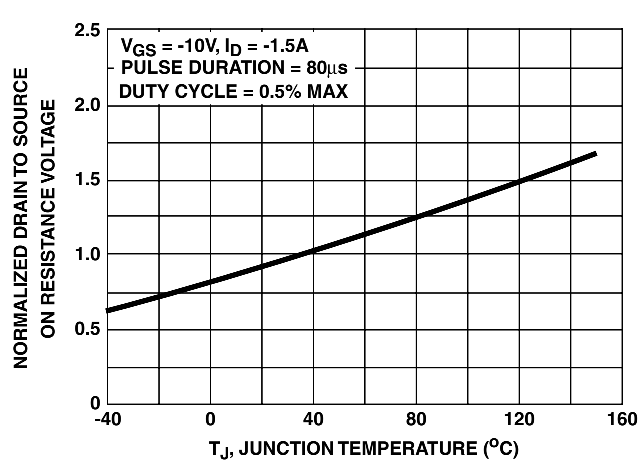


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

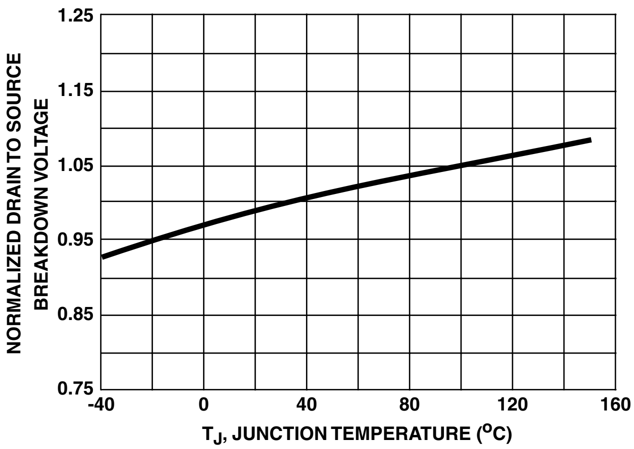


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

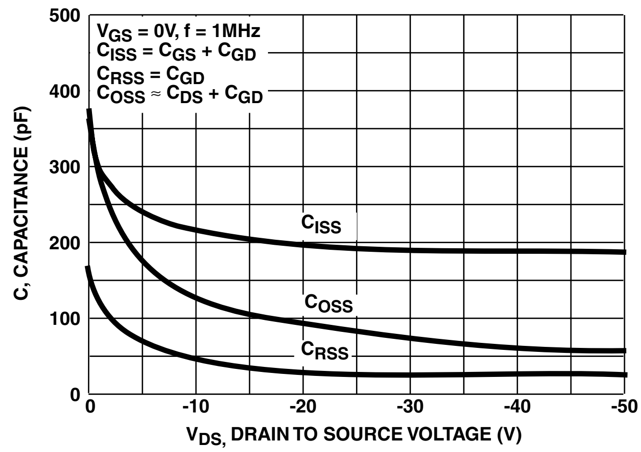


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

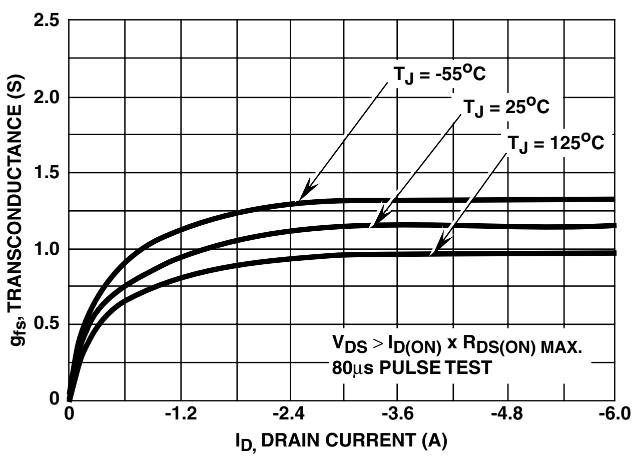


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

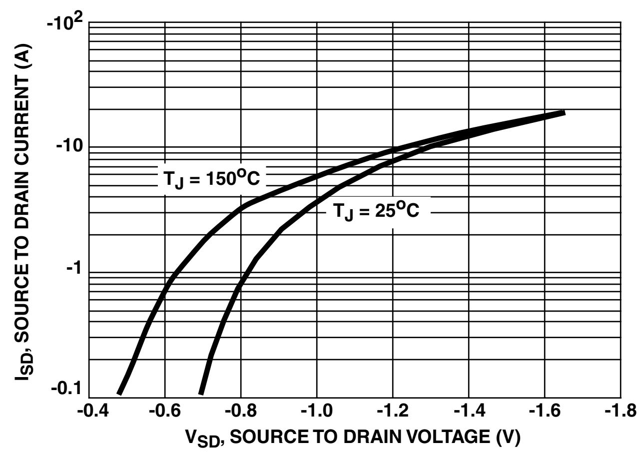


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

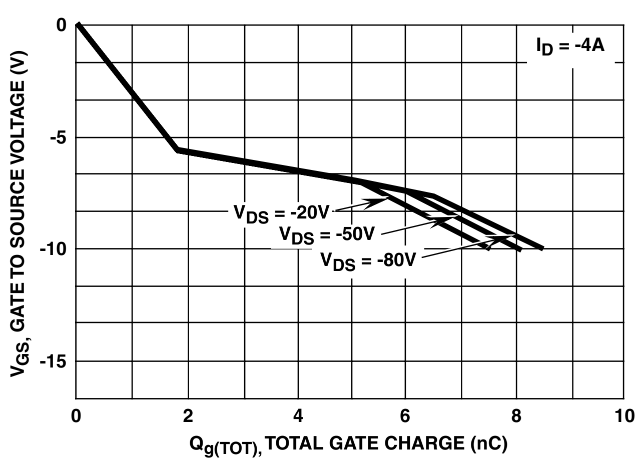


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

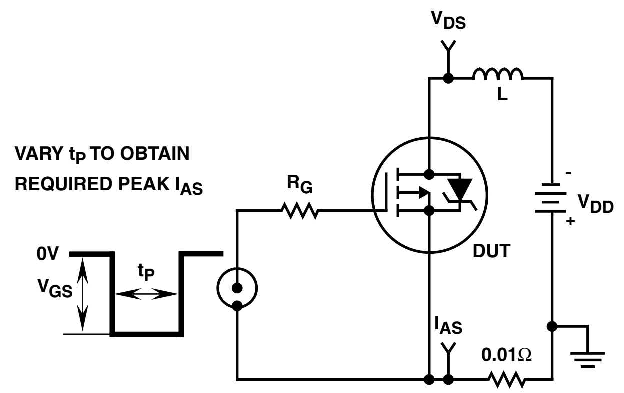


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

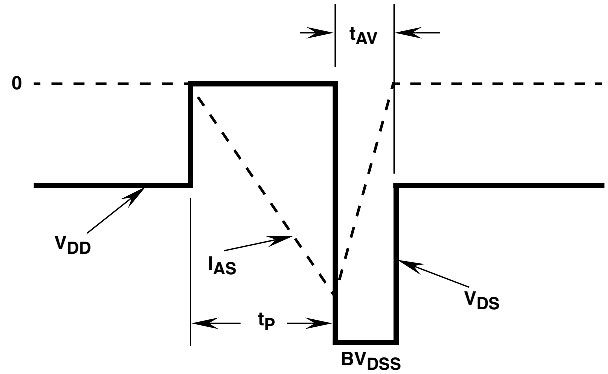


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

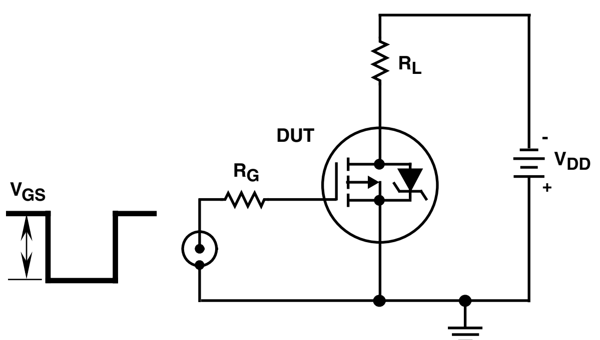


FIGURE 17. SWITCHING TIME TEST CIRCUIT

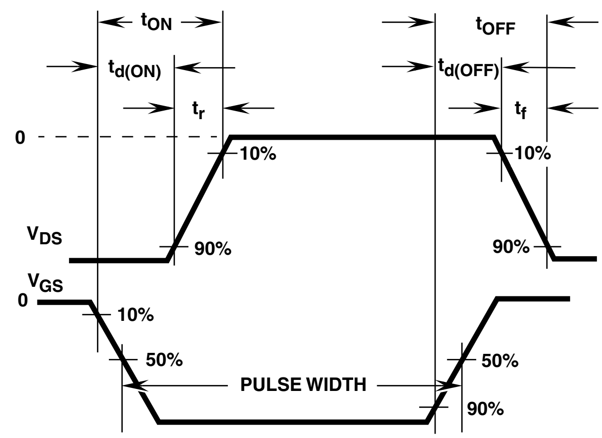


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

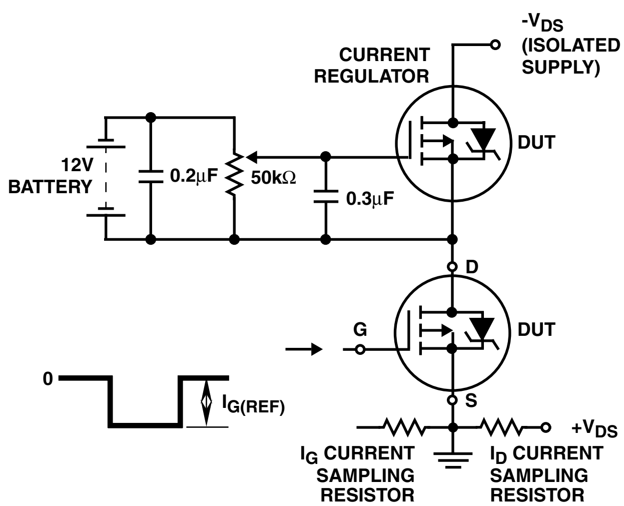


FIGURE 19. GATE CHARGE TEST CIRCUIT

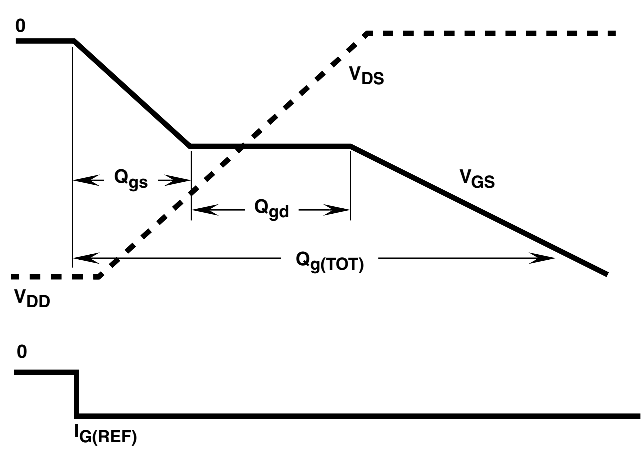


FIGURE 20. GATE CHARGE WAVEFORMS

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
Bottomless™
CoolFET™
CROSSVOLT™
DenseTrench™
DOME™
EcoSPARK™
E²CMOS™
EnSigna™
FACT™
FACT Quiet Series™
FAST ®
FASTr™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
ISOPLANAR™
LittleFET™
MicroFET™
MicroPak™
MICROWIRE™
OPTOLOGIC™
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerTrench®
QFET™
QS™
QT Optoelectronics™
Quiet Series™
SILENT SWITCHER®
SMART START™
STAR*POWER™
Stealth™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic™
TruTranslation™
UHC™
UltraFET®
VCX™

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4