



7N50

Preliminary

Power MOSFET

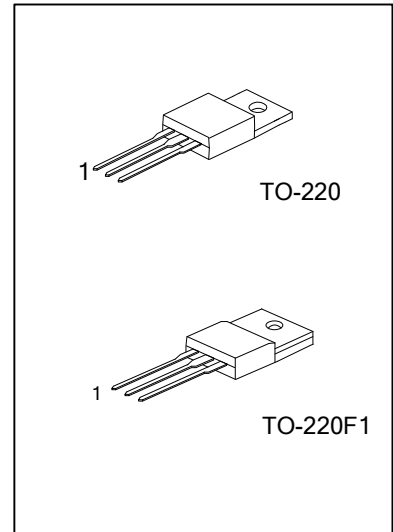
7 Amps, 500 Volts

N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **7N50** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

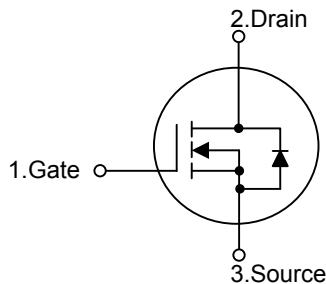
The UTC **7N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.



FEATURES

- * 7A, 500V, $R_{DS(ON)}=0.9\Omega$ @ $V_{GS}=10V$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N50L-TA3-T	7N50G-TA3-T	TO-220	G	D	S	Tube
7N50L-TF1-T	7N50G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7N50L-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Free</p>	<p>(1) T: Tube</p> <p>(2) TA3: TO-220 ,TF1: TO-220F1</p> <p>(3) G: Halogen Free, L: Lead Free</p>
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■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V _{DSS}	500	V
Gate-Source Voltage			V _{GSS}	±30	V
Drain Current	Continuous (T _C =25°C)		I _D	7 *	A
	Pulsed (Note 1)		I _{DM}	28 *	A
Avalanche Current (Note 1)			I _{AR}	7	A
Avalanche Energy	Single Pulsed (Note 2)		E _{AS}	270	mJ
	Repetitive (Note 3)		E _{AR}	8.9	mJ
Peak Diode Recovery dv/dt (Note 3)			dv/dt	4.5	V/ns
Power Dissipation	T _C =25°C	TO-220	P _D	89	W
		TO-220F1		39	
	Derate above 25°C	TO-220		0.71	W/°C
		TO-220F1		0.31	
Junction Temperature			T _J	+150	°C
Storage Temperature			T _{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

* Drain current limited by maximum junction temperature

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^\circ\text{C/W}$
	TO-220F1		62.5	
Junction to Case	TO-220	θ_{JC}	1.4	$^\circ\text{C/W}$
	TO-220F1		3.2	

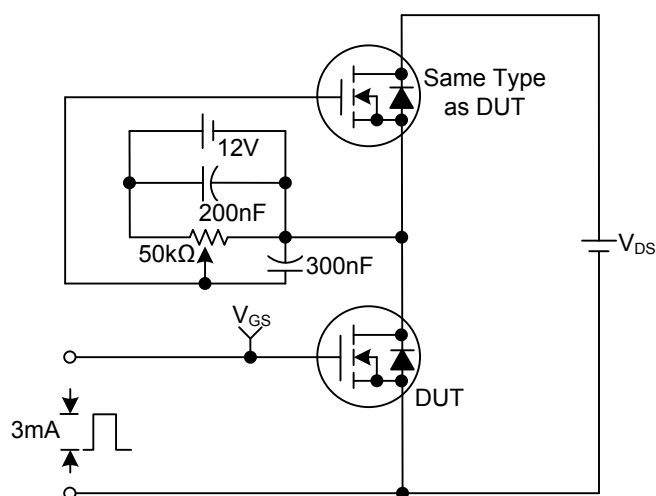
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	500			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=500V, V_{GS}=0V$			1	μA
			$V_{DS}=400V, T_C=125^{\circ}C$			10	
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+30V, V_{DS}=0V$			+100	nA
	Reverse		$V_{GS}=-30V, V_{DS}=0V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10V, I_D=3.5A$		0.76	0.9	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$		720	940	pF
Output Capacitance		C_{OSS}			95	190	pF
Reverse Transfer Capacitance		C_{RSS}			9	13.5	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	$V_{GS}=10V, V_{DS}=400V, I_D=7A$ (Note 4, 5)		12.8	16.6	nC
Gate to Source Charge		Q_{GS}			3.7		nC
Gate to Drain Charge		Q_{GD}			5.8		nC
Turn-ON Delay Time		$t_{D(ON)}$	$V_{DD}=250V, I_D=7A, R_G=25\Omega$ (Note 4, 5)		6	20	ns
Rise Time		t_R			55	120	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			25	60	ns
Fall-Time		t_F			35	80	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				7	A
Maximum Body-Diode Pulsed Current		I_{SM}				28	A
Drain-Source Diode Forward Voltage		V_{SD}	$I_S=7A, V_{GS}=0V$			1.4	V
Body Diode Reverse Recovery Time		t_{RR}	$I_S=7A, V_{GS}=0V, dI_F/dt=100A/\mu s$		275		ns
Body Diode Reverse Recovery Charge		Q_{RR}	(Note 4)		0.04		μC

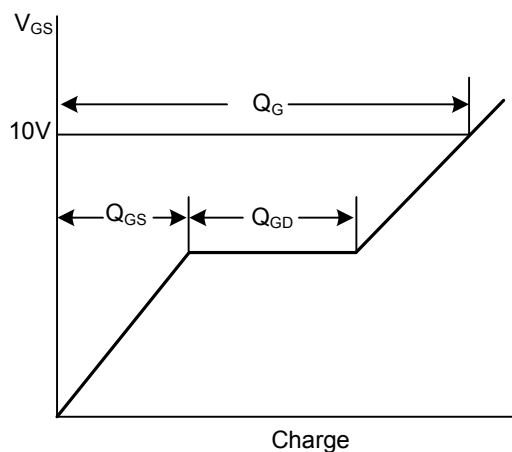
- Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature
 2. $L = 10\text{mH}$, $I_{AS} = 7\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
 3. $I_{SD} \leq 7\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
 4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
 5. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

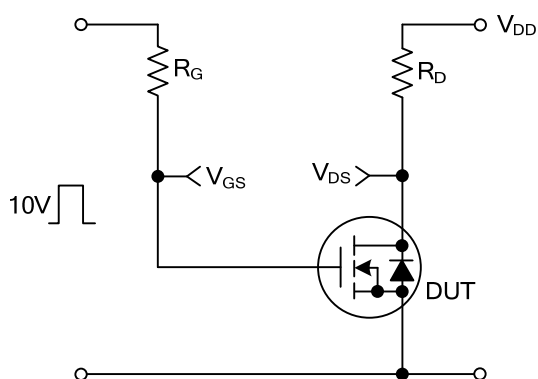
Gate Charge Test Circuit



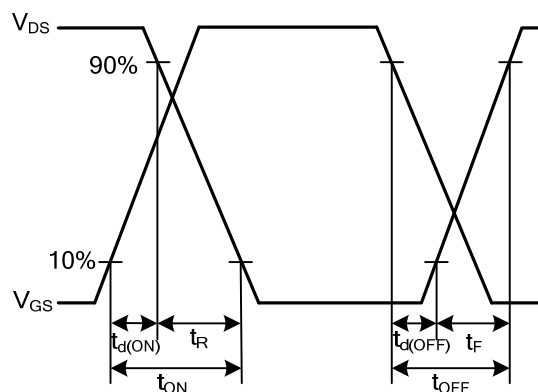
Gate Charge Waveforms



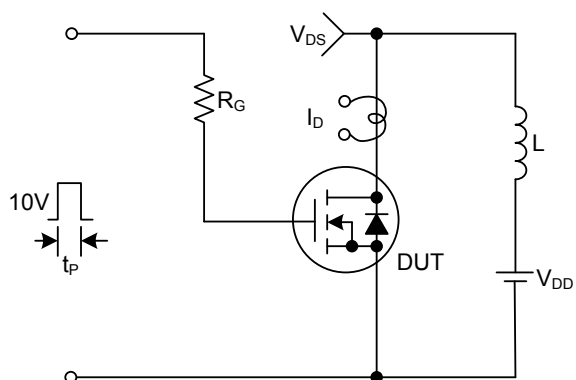
Resistive Switching Test Circuit



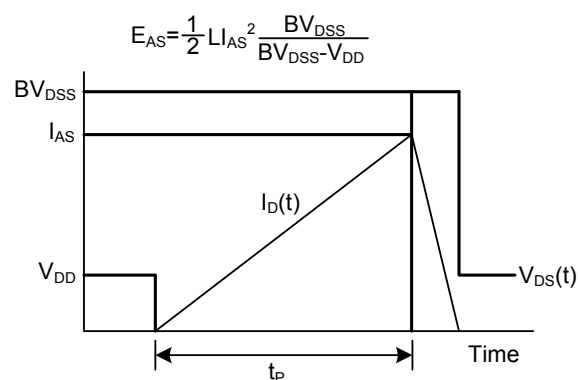
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



dv/dt controlled by R_G
 I_{SD} controlled by pulse period



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