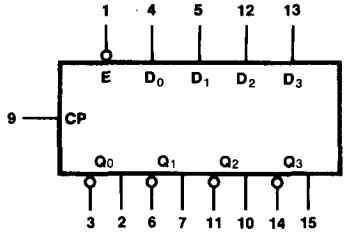
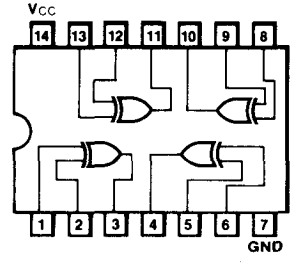
DIGITAL - TTL

D93
54LS/74LS379

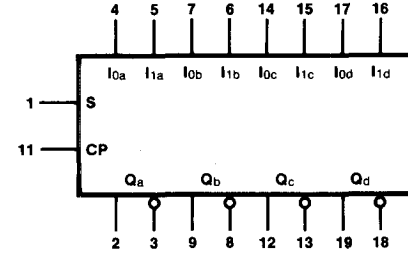


V_{CC} = Pin 16
GND = Pin 8

D94
9386, 74LS266, 54LS/74LS386

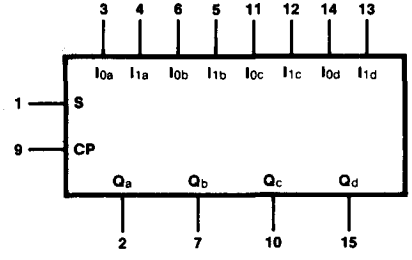


D95
54LS/74LS398



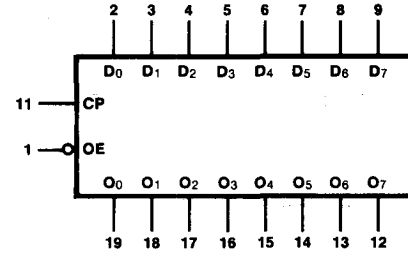
V_{CC} = Pin 20
GND = Pin 10

D96
54LS/74LS399



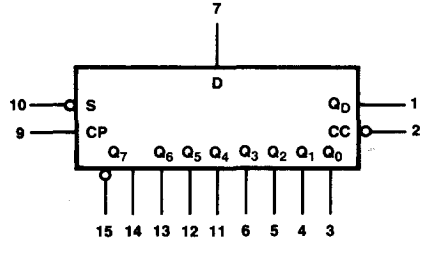
V_{CC} = Pin 16
GND = Pin 8

D97
54LS/74LS574



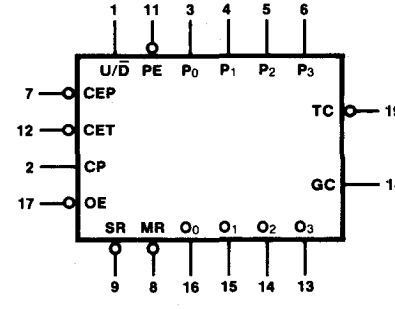
V_{CC} = Pin 20
GND = Pin 10

D98
54LS/74LS502



V_{CC} = Pin 16
GND = Pin 8

D99
54LS/74LS568,
54LS/74LS569



V_{CC} = Pin 20
GND = Pin 10

TTL

REGISTERS (Cont'd)

Item	Function	DEVICE NO.	No. of Bits	Serial Entry	Parallel Entry No. of Bits[1]	Clock Edge	Max Clock Freq MHz (Typ)	Clock to Output Delay-ns (Typ)	Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
1	Parallel-in/Parallel-out	**54LS/74LS399**	4	—	2D Mux	⎍	35	20	37	D96	4L,6B,9B
2	Parallel-in/Parallel-out	**54LS[3]/74LS574**	8	—	8S	⎍	55	20	135	D97	9Z
3	Parallel-in/Serial-out	**54/7494**	4	D	4S	⎍	10	25	175	D165	4L,7B,9B
4	Parallel-in/Serial-out	**54/74165**	8	D	8A	⎍	26	19	210	D175	4L,7B,9B
5	Parallel-in/Serial-out	**54/74166**	8	D	8S	⎍	35	20	360	D176	4L,7B,9B
6	Parallel-in/Serial-out	**54LS/74LS165**	8	D	8A	⎍	40	19	105	D175	4L,7B,9B
7	Parallel-in/Parallel-out Shift Right	**54LS/74LS95B**	4	D	4S	⎍	35	20	65	D166	3I,6A,9A
8	Parallel-in/Parallel-out Shift Right	**54LS/74LS195**	4	J,K	4S	⎍	39	17	70	D163	4L,6B,9B
9	Parallel-in/Parallel-out Shift Right	**54LS/74LS295A**	4	D	4S	⎍	28	40	75	D171	3I,6A,9A
10	Serial-in/Serial-out	**9328**	16	2x2D Mux	—	⎍	30	17	300	D177	4L,7B,9B
11	Serial-in/Serial-out	**93L28**	16	2x2D Mux	—	⎎	15	42	80	D177	4L,7B,9B
12	Serial-in/Serial-out	**54/7491**	8	2D	—	⎎	18	25	175	D178	3I,7A,9A
13	Multiport Registers	**9338**	8	D	—	⎎	25	23	425	D153	4L,7B,9B
14	Multiport Registers	**93L38**	8	D	—	⎍	20	38	105	D153	4L,7B,9B
15	Multiport Registers	**54/74170**	16	—	4A	⎎	—	25	635	D154	4L,7B,9B
16	Multiport Registers	**54LS/74LS170**	16	—	4A	⎍	—	25	125	D154	4L,7B,9B
17	Multiport Registers	**54LS/74LS670**	16	—	4A	⎍	—	30	150	D154	4L,7B,9B
18	Quad D (3S)[2]	**54/74173**	4	—	4S	⎍	35	28	250	D189	4L,7B,9B
19	Quad D (3S)[2]	**54LS/74LS173**	4	—	4S	⎍	30	18	35	D189	4L,7B,9B
20	Successive Approx Register	**54LS/74LS502**	8	D	—	⎍	25	18	325	D98	4I,6B,9B

1. A = asynchronous, S = synchronous
2. 3S = 3-state
3. To be announced