

SN54167, SN74167 SYNCHRONOUS DECADE RATE MULTIPLIERS

DECEMBER 1972 — REVISED MARCH 1988

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 MHz

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These decade counters feature buffered clock, clear, enable and set-to-nine inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe set-to-nine, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 10, i.e.:

$$f_{out} = \frac{M \cdot f_{in}}{10}$$

where: $M = B_3 \cdot 2^3 + B_2 \cdot 2^2 + B_1 \cdot 2^1 + B_0 \cdot 2^0$
for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform two-decade rate multiplication (0-99), the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output. For longer words, see typical application data, Figure 1.

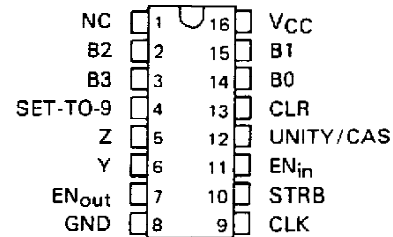
The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the output. These devices are completely compatible with most TTL and DTL families. Typical dissipation is 270 milliwatts. The SN54167 is characterized for operation over the full military temperature range of -55°C to 125°C , and the SN74167 is characterized for operation from 0°C to 70°C .

SN54167 . . . J OR W PACKAGE

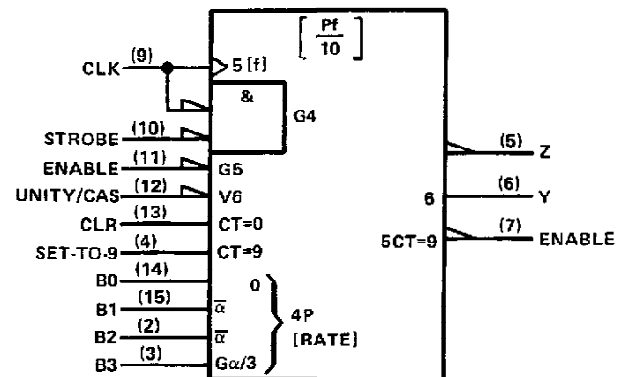
SN74167 . . . N PACKAGE

(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

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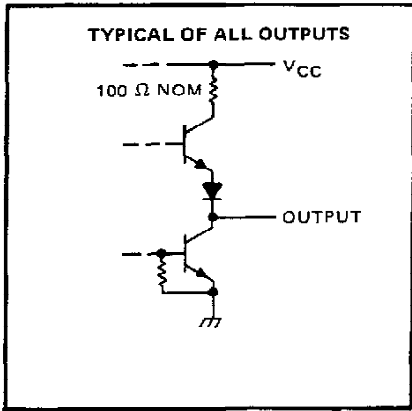
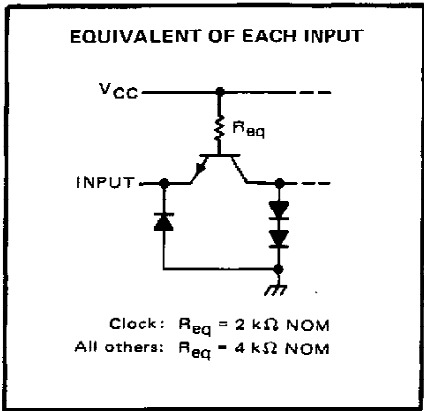
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STATE AND/OR RATE FUNCTION TABLE (See Note A)

INPUTS								OUTPUTS			NOTES	
CLEAR	ENABLE	STROBE	BCD RATE				NUMBER OF CLOCK PULSES	UNITY/ CASCADE	LOGIC LEVEL OR NUMBER OF PULSES			
									Y	Z		ENABLE
H	X	H	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	C
L	L	L	L	L	L	H	10	H	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	C
L	L	L	L	L	H	H	10	H	3	3	1	C
L	L	L	L	H	L	L	10	H	4	4	1	C
L	L	L	L	H	L	H	10	H	5	5	1	C
L	L	L	L	H	H	L	10	H	6	6	1	C
L	L	L	L	H	H	H	10	H	7	7	1	C
L	L	L	L	H	L	L	10	H	8	8	1	C
L	L	L	L	H	L	H	10	H	9	9	1	C
L	L	L	H	L	H	L	10	H	8	8	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	E

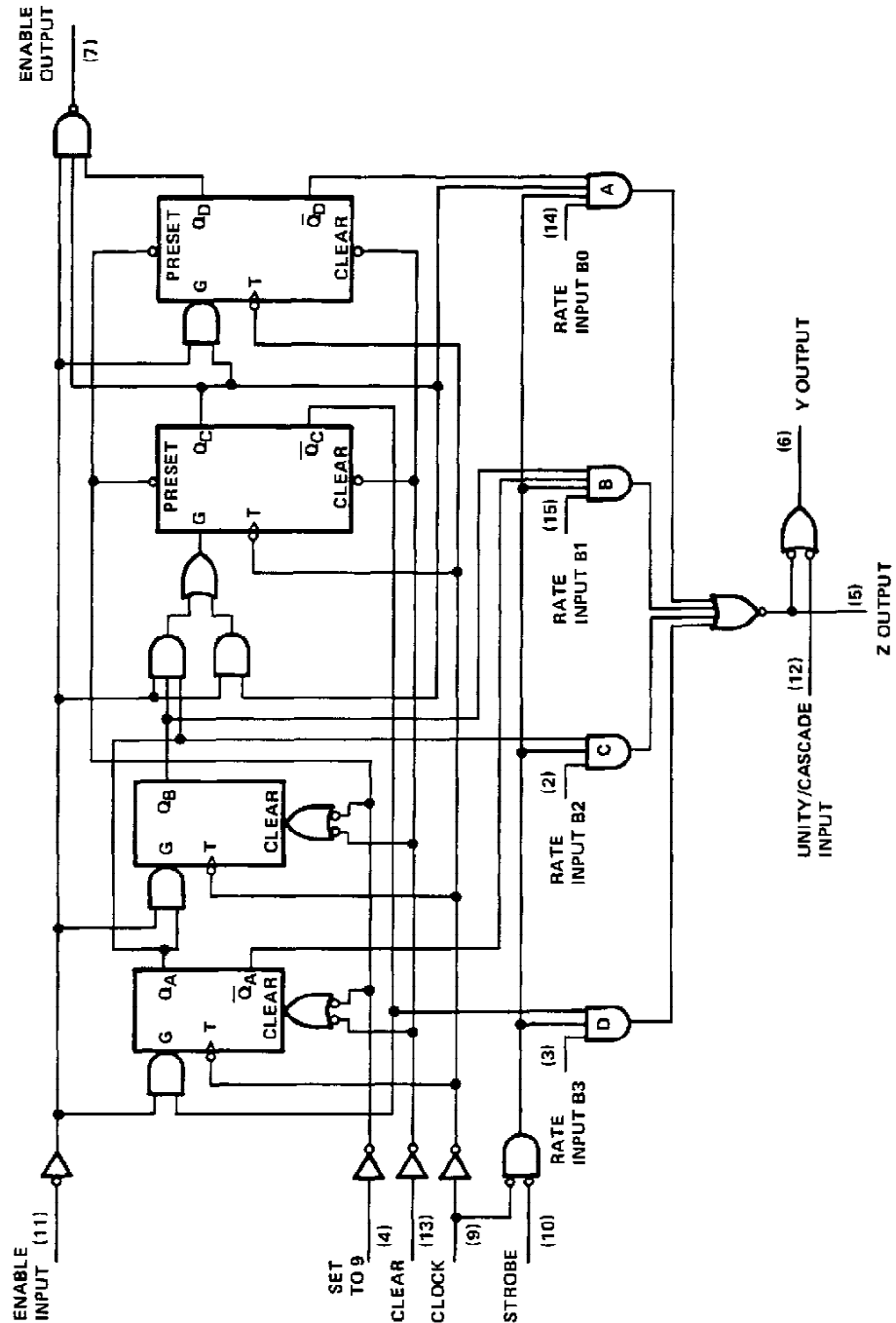
- NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
D. These input conditions exceed the range of the decimal rate inputs.
E. Unity/cascade can be used to inhibit output Y.

schematics of inputs and outputs



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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54167	-55°C to 125°C
SN74167	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54167			SN74167			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Width of set-to-nine pulse $t_{w(set-to-9)}$	15			15			ns
Enable setup time, t_{SU} : From positive-going transition of clock pulse From negative-going transition of previous clock pulse	25 0		$t_{w(clock)}-10$	25 0		$t_{w(clock)}-10$	ns ns
Enable hold time, t_H : From positive-going transition of clock pulse From negative-going transition of previous clock pulse	0 20	$t_{w(clock)}-10$ $t_{cp}-10$		0 20	$t_{w(clock)}-10$ $t_{cp}-10$		ns ns
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 2: $t_{w(clock)}$ is the interval in which the clock is high. t_{cp} is the total clock cycle starting with a negative transition. See Figure 1 on SN5497, SN7497 data sheet.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	clock input			80	μ A
		other inputs			40	μ A
I_{IL}	Low-level input current	clock inputs			-3.2	mA
		other inputs			-1.6	mA
I_{OS}	Short circuit output current§	$V_{CC} = \text{MAX}$	-18		-55	mA
I_{CCH}	Supply current, output high	$V_{CC} = \text{MAX}$, See Note 3		43		mA
I_{CCL}	Supply current, output low	$V_{CC} = \text{MAX}$, See Note 4		65	99	mA

NOTES: 3. I_{CCH} is measured with outputs open and all inputs low.

4. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input which is low.

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETERS†	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 400 Ω, See Note 5	25	32		MHz
t _{PLH}	Enable	Enable			13	20	ns
t _{PHL}					14	21	
t _{PLH}	Strobe	Z			12	18	ns
t _{PHL}					15	23	
t _{PLH}	Clock	Y			26	39	ns
t _{PHL}					20	30	
t _{PLH}	Clock	Z			12	18	ns
t _{PHL}					17	26	
t _{PLH}	Rate	Z			9	14	ns
t _{PHL}					6	10	
t _{PLH}	Unity/Cascade	Y			9	14	ns
t _{PHL}					6	10	
t _{PLH}	Strobe	Y			19	30	ns
t _{PHL}					22	33	
t _{PLH}	Clock	Enable			19	30	ns
t _{PHL}					22	33	
t _{PLH}	Clear	Y			24	36	ns
t _{PHL}		Z			15	23	
t _{PHL}	Set-to-9	Enable			18	27	ns
t _{PLH}	Any Rate Input	Y		15	23	ns	
t _{PHL}					15		23

† $f_{\max}$ is maximum clock frequency.

t_{PLH} is propagation delay time, low-to-high-level output.

t_{PHL} is propagation delay time, high-to-low-level output.

NOTE 5: Load circuit, voltage waveforms, and input conditions for measuring switching characteristics are the same as those for the SN5497 and SN7497.

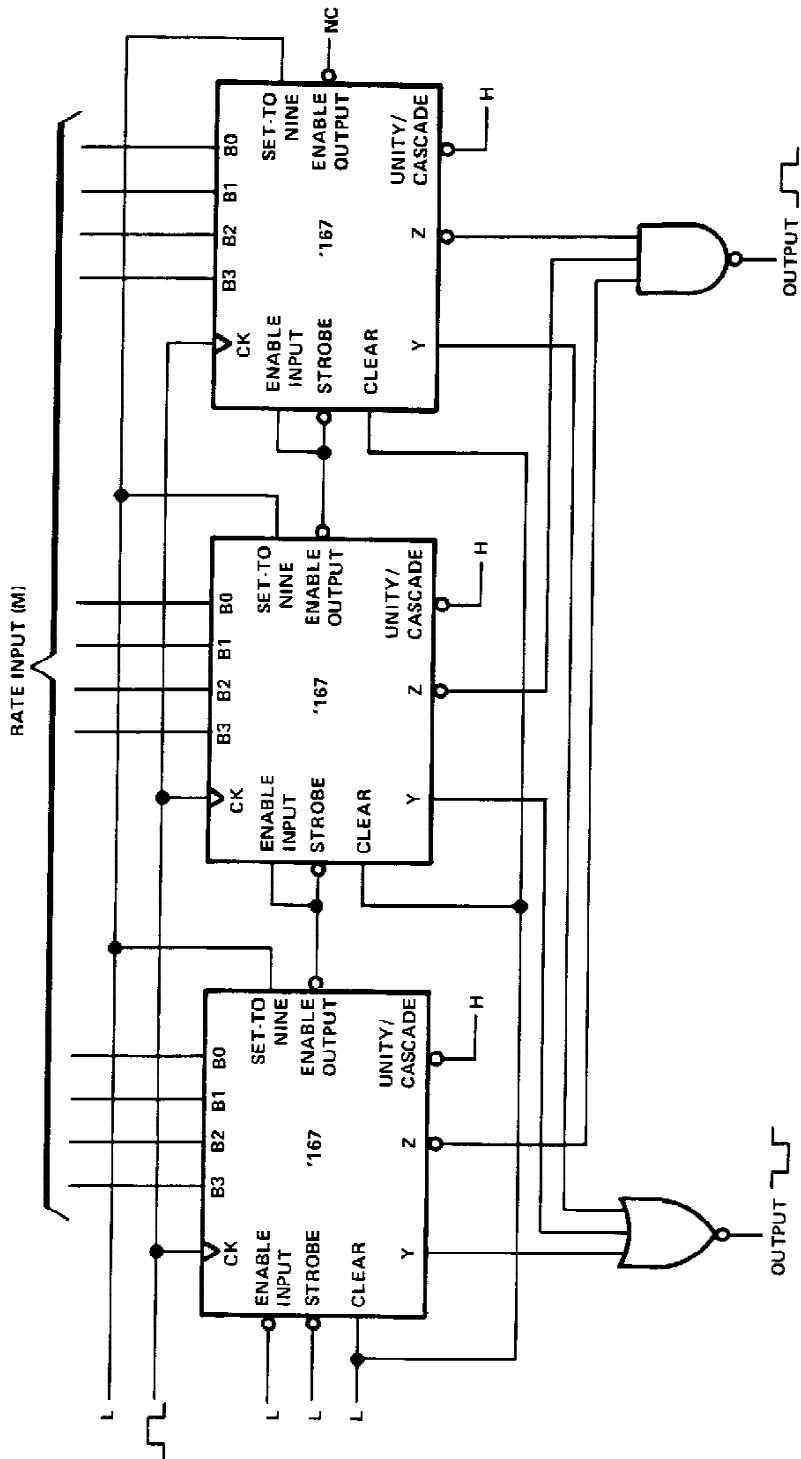

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TYPICAL APPLICATION DATA

This application demonstrates how the decimal-rate multipliers may be cascaded for longer words. Three decades are illustrated (0.999 to 999) although longer words can be implemented by using the pattern shown. The output is decoded either from output Y with a NOR gate or from output Z with a NAND gate. Either method of decoding produces the complement of the output used.



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