ADVANCED INFORMATION

C-MOS 4000 SERIES

DESCRIPTION

The 4013 consists of two identical independent delay-type flip-flops. Each flip-flop has independent data, set, reset, clock inputs and Q and $\overline{Q}$ outputs. The 4013 can be used for shift register applications, or by connecting $\overline{Q}$ back to the "D" input, for counter and toggle applications.

The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting and resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

FEATURES

- 10Mz TYPICAL TOGGLE RATE
- WIDE OPERATING VOLTAGE RANGE: +3V to +15V
- HIGH NOISE IMMUNITY: 45% OF POWER SUPPLY VOLTAGE
- EXTREMELY LOW POWER DISSIPATION: TYPICALLY 50nW QUIESCENT
- EXCELLENT TEMPERATURE STABILITY
- INPUTS PROTECTED FOR STATIC CHARGE
- HIGH INPUT IMPEDANCE: TYPICALLY 10^{12} OHMS
- LOW OUTPUT IMPEDANCE:
  HIGH: TYPICALLY 400 OHMS
  LOW: TYPICALLY 200 OHMS
- WIDE TEMPERATURE RANGE −40°C to +85°C AND −55°C to +125°C

APPLICATIONS

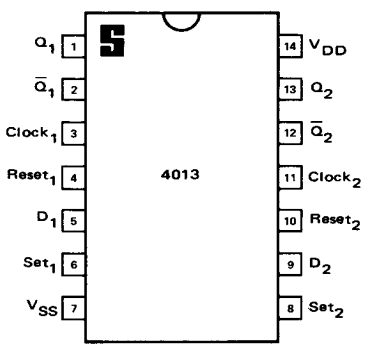
DATA TERMINALS
INSTRUMENTATION
APPLIANCES
INDUSTRIAL CONTROLS
COMPUTERS
CALCULATORS
COMMUNICATION EQUIPMENT
HAND-HELD INSTRUMENTS

PART IDENTIFICATION

TYPE	FUNCTION	TEMP./PKG
4013	DUAL "D" FLIP-FLOP	N/A, S/F, S/Q

PIN CONFIGURATION

A, F, Q PACKAGES



MAXIMUM GUARANTEED RATINGS

Operating Ambient Temperature	
"N"	−40°C to +85°C
"S"	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Inputs with Respect to V_{SS}	$V_{SS} \leq V_I \leq V_{DD}$
DC Voltage Supply Range	−0.5V to +15V
Device Dissipation (per pkg.)	200mW
Recommended DC Supply Voltage	3V to 15V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	S4013 LIMITS									UNITS	TEST CONDITIONS		
		−55°C			25°C			125°C					V_O VOLTS	V_{DD} VOLTS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
Quiescent Device Current	I_L			1 2		0.005 0.005	1 2			60 120	μA			5 10
Quiescent Device Dissipation/Pkg.	P_D			5 20		0.025 0.05	5 20			300 1200	μW			5 10
Output Voltage Low-Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V			5 10
High-Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V			5 10
Threshold Voltage: N-Channel	V_{THN}		1.7			1.5			1.3		V	I_D = 10μA		
P-Channel	V_{THP}		−1.7			−1.5			−1.3		V	I_D = −10μA		
Noise Immunity (All inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V		0.8 1.0	5 10
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V		4.2 9.0	5 10
Output Drive Current N-Channel	I_DN	0.65 1.25			0.5 1	1 2.5		0.35 0.75			mA		0.5 0.5	5 10
P-Channel	I_DP	−0.31 −0.8			−0.25 −0.65	−0.5 −1.3		−0.175 −0.45			mA		4.5 9.5	5 10
Input Current	I_I					10					pA			

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	N4013 LIMITS									UNITS	TEST CONDITIONS		
		−40°C			25°C			85°C					V_O VOLTS	V_{DD} VOLTS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
Quiescent Device Current	I_L			10 20		0.01 0.02	10 20			140 280	μA			5 10
Quiescent Device Dissipation/Pkg.	P_D			50 200		0.05 0.2	50 200			700 2800	μW			5 10
Output Voltage Low-Level	V_{OL}			0.01 0.01		0 0	0.01 0.01			0.05 0.05	V			5 10
High-Level	V_{OH}	4.99 9.99			4.99 9.99	5 10		4.95 9.95			V			5 10
Threshold Voltage N-Channel	V_{THN}		1.7			1.5			1.3		V	I_D = 10μA		
P-Channel	V_{THP}		−1.7			−1.5			−1.3		V	I_D = −10μA		
Noise Immunity (All inputs)	V_{NL}	1.5 3			1.5 3	2.25 4.5		1.4 2.9			V		0.8 1.0	5 10
	V_{NH}	1.4 2.9			1.5 3	2.25 4.5		1.5 3			V		4.2 9.0	5 10
Output Drive Current N-Channel	I_DN	0.35 0.72			0.3 0.6	1 2.5		0.24 0.5			mA		0.5 0.5	5 10
P-Channel	I_DP	−0.17 −0.4			−0.14 −0.33	−0.5 −1.3		0.605 −0.27			mA		4.5 9.5	5 10
Input Current	I_I					10					pA			

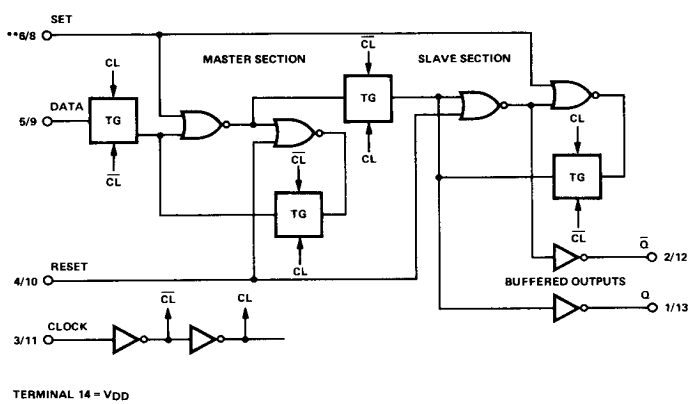
DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$ $C_L = 15pF$, and input rise and fall times = 20ns except t_r CL, t_f CL. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

CHARACTERISTICS	SYMBOLS	LIMITS						UNITS	TEST CONDITIONS	
		S4013			N4013					V_{DD} VOLTS
		MIN.	TYP.	MAX.	MIN.	MAX.	TYP.			
CLOCKED OPERATION										
Propagation Delay Time:	$t_{PHL} = t_{PLH}$		150 75	300 110		150 75	350 125	ns		5 10
Transition Time	$t_{THL} = t_{TLH}$		75 50	125 70		75 50	150 75	ns		5 10
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		125 50	200 80		125 50	500 100	ns		5 10
Clock Rise & Fall Time	$*t_{rCL} = t_{fCL}$			15 5			15 5	μs		5 10
Set Up Time			20 10	40 20		20 10	50 25	ns		5 10
Maximum Clock Frequency	f_{CL}	2.5 7	4 10		1 5	4 10		MHz		5 10
Input Capacitance	C_I		5			5		pF	Any Input	
SET AND RESET OPERATION										
Propagation Delay Time	$t_{PHL(R)} = t_{PLH(R)}$		175 75	300 110		175 75	350 125	ns		5 10
Minimum Set and Reset Pulse Widths	$t_{WH(S)}$, $t_{WH(R)}$		125 50	250 100		125 50	500 125	ns		5 10

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

LOGIC DIAGRAM



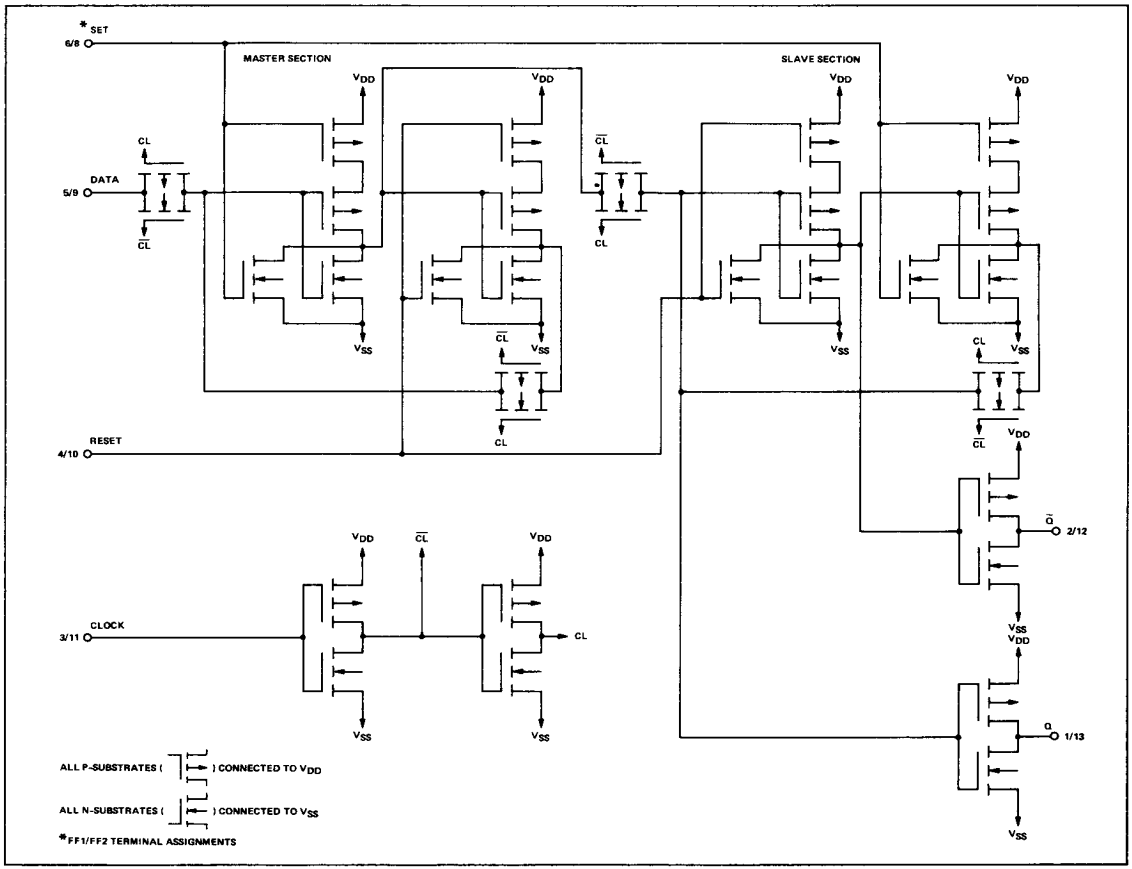
TERMINAL 14 = V_{DD}
TERMINAL 7 = GND

TRUTH TABLE

CL▲	D	R	S	Q	$\bar{Q}$	
⌒	0	0	0	0	1	
⌒	1	0	0	1	0	
⌣	x	0	0	Q	$\bar{Q}$	NO CHANGE
x	x	1	0	0	1	
x	x	0	1	1	0	
x	x	1	1	*	*	

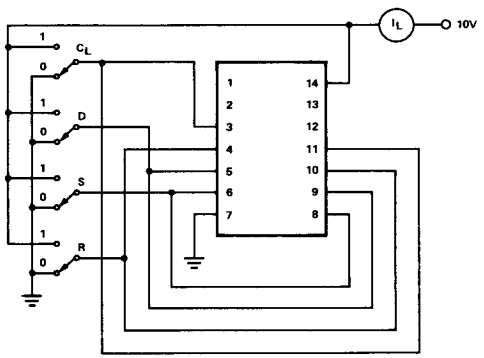
* INVALID CONDITION
** FF1/FF2 TERMINAL ASSIGNMENTS
▲ LEVEL CHANGE
x DON'T CARE

SCHEMATIC DIAGRAM



TEST CIRCUITS

QUIESCENT DEVICE CURRENT TEST CIRCUIT



TEST PERFORMED WITH THE FOLLOWING SEQUENCE OF "1's" AND "0's".

C_L	S	D	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

NOISE IMMUNITY TEST CIRCUIT